

# Notice of Allowability

Application No.

09/656,550

Examiner

Mujtaba K Chaudry

Applicant(s)

CHREN, JR., WILLIAM A

Art Unit

2133

## -- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 10/13/2004.
2. ☒ The allowed claim(s) is/are 1-26.
3. ☒ The drawings filed on 13 October 2004 are accepted by the Examiner.
4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a) ☐ All    b) ☐ Some\*    c) ☐ None    of the:
    1. ☐ Certified copies of the priority documents have been received.
    2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
    3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
  6. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
    - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
      - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date \_\_\_\_\_.
    - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

### Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date \_\_\_\_\_
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date \_\_\_\_\_
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other \_\_\_\_\_

*[Signature]*  
\_\_\_\_\_  
2004 OCT 13

### **REASONS FOR ALLOWANCE**

Claims 1-26 are allowed. The following is an Examiner's statement of reasons for allowance:

Independent claim 1 of the present application teaches a arithmetic circuit with built-in self testing of input-to-output delay for use with a Residue Number System (RNS), said arithmetic circuit comprising: an arithmetic core for performing an RNS arithmetic operation, the arithmetic core having an output and at least two inputs; input-to-output delay test circuitry coupled to the arithmetic core, the input-to-output delay test circuitry selectively feeding the output of the arithmetic core back to at least one of the inputs without latching so as to induce natural oscillation at the output of the arithmetic core during testing of the input-to-output delay; and input-to-output delay logic circuitry coupled to the output of the arithmetic core, the input-to-output delay logic circuitry measuring an oscillation frequency of the output of the arithmetic core during testing of the input-to-output delay, making a determination of whether the oscillation frequency that is measured is at least equal to a minimum threshold value, and producing a pass signal or a fail signal based on the determination that is made in order to indicate whether or not the input-to-output delay of the arithmetic core is within specification. The foregoing limitations are not found in the prior arts of record.

The prior art of record, namely Chren (USPN 5430764), teaches a direct digital frequency synthesizer employs residue number system based processors to generate output waveforms of desired frequencies. The frequency synthesizer includes a phase accumulator comprising a plurality of individual adders, each adding a predefined quantity to a digit of a frequency setting word in which the individual digits are residue digits of differing moduli. The outputs of the independent adders form a combined residue output word which is used to address

Art Unit: 2133

a memory storing signal samples. In one embodiment, the memory is a dual port ROM storing samples of one-quarter of a sine wave and the dual port ROM is simultaneously addressed to read a selected sample and an associated sample corresponding to the magnitude of a sample of the sine wave advanced by 90.degree. from the first sample. A sample select logic circuit selects one of the outputs of the dual port memory on the basis of selected bits of the combined residue word and data bits stored in the ROM with the samples to select and determine the sign of the sample of the sine wave. In another embodiment, the memory comprises a plurality of independent memories, corresponding to the number of independent adders, each storing residue information and a residue processing array processes the residue data obtained from the independent memories and provides a residue encoded signal to a residue-to-analog converter which generates the desired analog output.

None of the prior arts of record teach nor fairly suggest all the limitations in the independent claim 1 of the present application. In particular, the limitations of a arithmetic circuit with built-in self testing of input-to-output delay for use with a Residue Number System (RNS) wherein the arithmetic circuit comprises an arithmetic core for performing an RNS arithmetic operation having an output and at least two inputs; input-to-output delay test circuitry coupled to the arithmetic core, the input-to-output delay test circuitry selectively feeding the output of the arithmetic core back to at least one of the inputs without latching so as to induce natural oscillation at the output of the arithmetic core during testing of the input-to-output delay; and input-to-output delay logic circuitry coupled to the output of the arithmetic core, the input-to-output delay logic circuitry measuring an oscillation frequency of the output of the

Art Unit: 2133

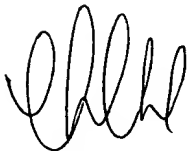
arithmetic core during testing of the input-to-output delay, making a determination of whether the oscillation frequency that is measured is at least equal to a minimum threshold value, and producing a pass signal or a fail signal based on the determination that is made in order to indicate whether or not the input-to-output delay of the arithmetic core is within specification are not taught nor fairly suggested in the prior arts of record.

Independent claims 10 and 18 include similar limitations of independent claim 1 and therefore are allowed for similar reasons.

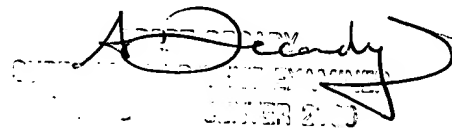
Dependent claims 2-9, 11-17 and 19-26 depend from independent claims 1, 10 and 18 and inherently include limitations therein and therefore are allowed as well.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 571-272-3817. The examiner may normally be reached Mon – Thur 6:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 571-272-3819.



Mujtaba Chaudry  
Art Unit 2133  
November 15, 2004



ALBERT DECADY  
SUPERVISOR  
ART UNIT 2133